Precise and effective scientific calculation on the CELL processor

Nguyen Hong Diep, **Stef Graillat**, and **Jean-Luc Lamotte**

LIP6/CNRS UMR 7606 (Laboratoire Informatique de Paris 6)
UPMC (Université Pierre et Marie Curie), Paris, France

Abstract

The CELL processor [1] jointly developed by Sony, Toshiba, and IBM provides a great potential for scientific computing with a peak performance in single precision of 204.8 Gflop/s. But, this performance is obtained with an SIMD processor which uses single precision floating numbers with a rounding mode toward zero. The goal of our work is to develop extended precision library for this architecture.

In this paper, we will study how to implement the double working precision library, named double-single on the SPEs (Synergistic Processing Element) which are the workhorse processors of the CELL. The approach is near from those used in [2] for the quad-double precision arithmetic. Firstly, algorithms based on error free transformations for the operators $(+, -, \times, /)$ are proposed for the rounding mode toward zero. We also prove their exactitude and we provide error limits on the precision of the double-single floating-point arithmetic.
The second part is devoted to the implementation on the SIMD processor by taking into account advantages of the characteristics of the SPE processor, among which the fully pipelined set of instructions in single precision and the FMA (Fused Multiply-Add) operator are the most important. We have managed to implement the error-free transformations very efficiently.

In the last part, the performance of our implementation are presented. Even though the theoretic peak performance of the library is much less than the performance of the double precision of the machine, which is about 2.7 Gflop/s in comparison with the 14.4 Gflop/s of the double precision, the results of our test show that it is not such that bad. When the 8 SPE are used to compute operations on very large vectors, the performance of the double-single and the true double floating point number are nearly equal.

In the future, with the same approach, we will promote our work to the quad-single precision. The quad-double precision will be reached with the next CELL processor which will provide a SIMD processor for double precision.

References

[1] J. A. Kahle, M. N. Day, H. P. Hofstee, C. R. Johns, T. R. Maeurer, and D. Shippy, Introduction to the Cell multiprocessor. *IBM J. Res. Dev.*, 49(4/5):589–604, 2005.
[2] Yozo Hida, Xiaoye S. Li, and David H. Bailey, Algorithms for quad-double precision floating point arithmetic. In *Proc. 15th IEEE Symposium on Computer Arithmetic*, pages 155–162. IEEE Computer Society Press, Los Alamitos, CA, USA, 2001.