Interval-Based Robust Statistical Techniques for Non-Negative Convex Functions, with Application to Timing Analysis of Computer Chips

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Overview

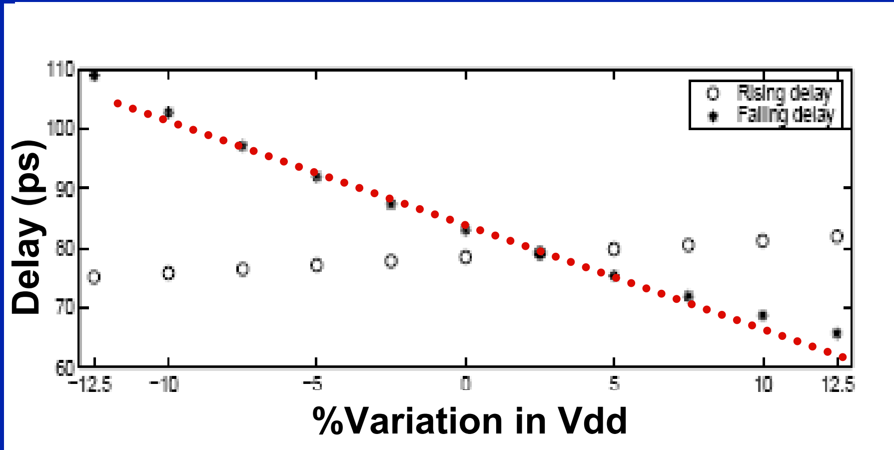
- Strategy of handling uncertainty: probabilistic interval analysis
- Timing analysis with partial probabilistic descriptions of uncertainty
  - Path delay computation
  - Circuit timing computation
- Experimental results
  - Robust timing estimates

Motivation

- Process and environmental uncertainty has great impact on timing performance of chip designs
  - Worst-case (interval) technique is conservative
  - Need to take into account probability
- Basic assumption of statistical timing analysis may not always be true: full probabilistic descriptions of parameters are not available
  - Only partial probabilistic information is available
- Need for strategy of handling partial probabilistic descriptions

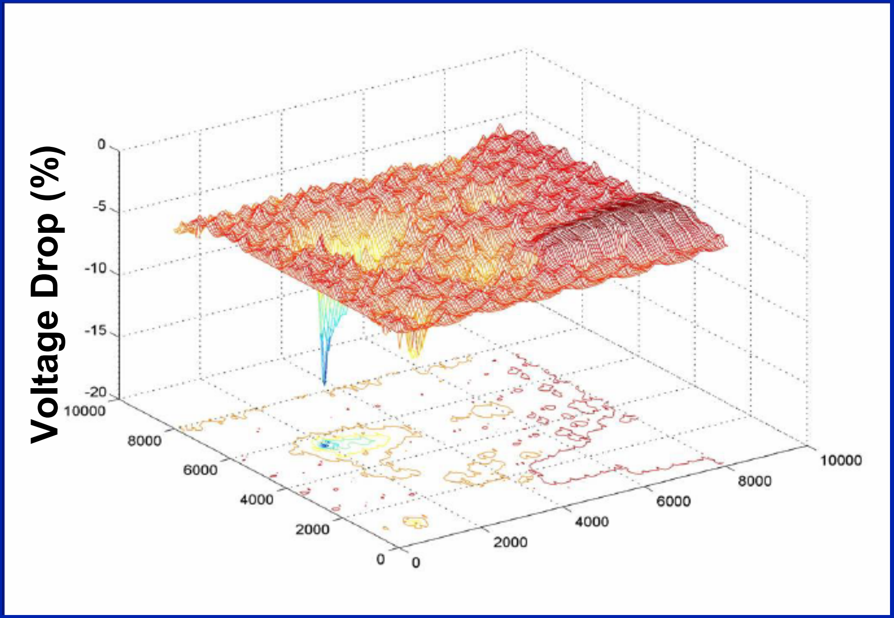
Limited Uncertainty Description

- Voltage drop affects gate delay
  - Difficult to fully characterize V_{dd} distribution
  - Use interval of V_{dd} to estimate worst/best-case delay



(Kouroussis '04)

- Mean and variance of voltage drop can be estimated
  - Use Monte Carlo sampling
  - Analytical technique also exists
  - Can compute moments – partial descriptions
  - Also can compute range



(Devgan)

Related Work

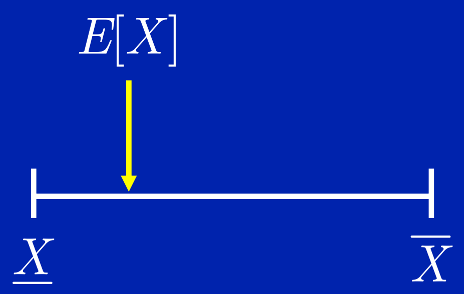
- Statistical Timing Analysis
  - Delay modeling: linear / nonlinear dependency on process variation
  - Process variability: Non-Gaussian Distribution (Zhan ’05; Chang ’05; Zhang ’05)

- Interval / affine methods
  - Interval analysis (Moore ’66)
  - Robust estimates using interval information

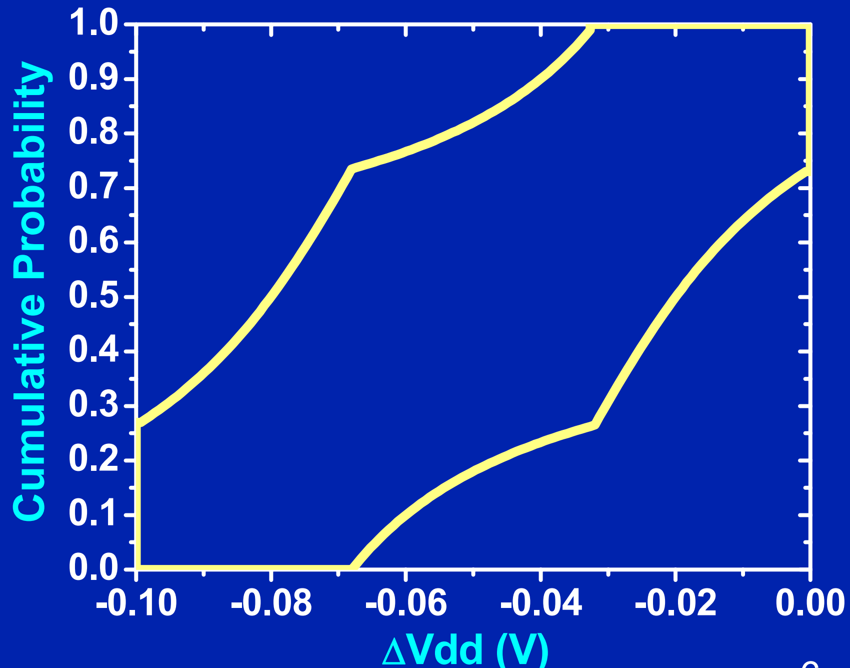
- Statistical delay computation based on affine arithmetic
  - Interconnect delay (Ma ’04)
  - Need assumption about distributions within intervals

Handling Probabilistic Interval Uncertainty

- Probabilistic interval analysis
  - Use moments (mean, variance) and range to estimate probabilistic bounds
  - Include notion of probability
  - Distribution-free

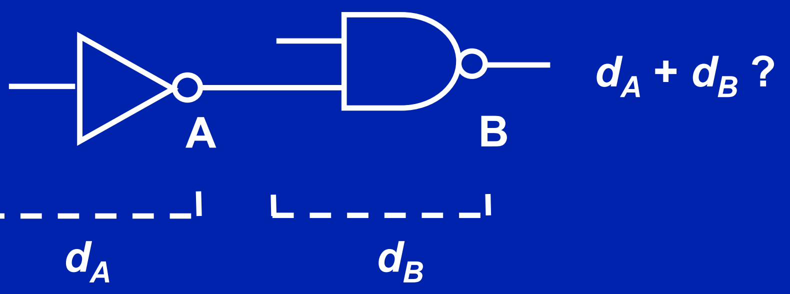


- Probability box: representation of partially-specified variables
  - A universal representation
  - Bounds for cumulative distribution functions
  - Knowledge of mean, variance, and interval permits constructing p-box

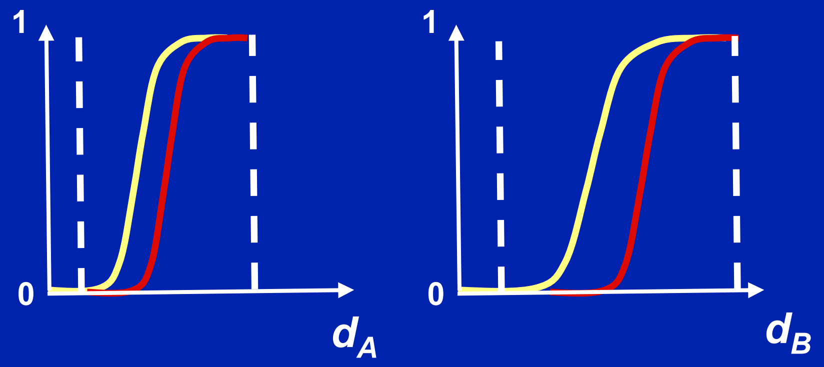


Operations of Probabilistic Interval Uncertainty in Timing Analysis

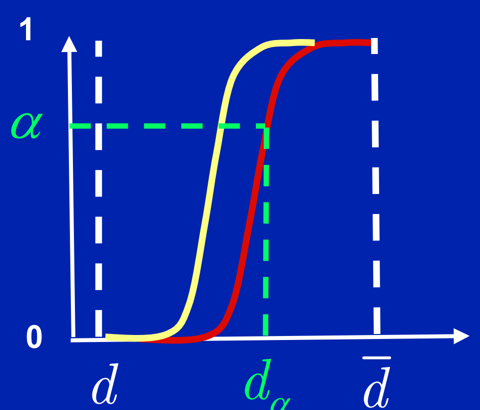
- Need to take into account correlation of gate delays



- Basic operations in timing analysis
  - Sum
  - Maximum



- Lower bound of cumulative probability (upper bound of delay) is a more important metric in timing analysis



Timing Analysis with Partial Probabilistic Descriptions of Parameters

- **Gate delay model**
  - **Consider global (die-to-die) and local (within-die) components**

$$d_i = \mu_i + \sum_{j=1}^{n} a_{i,j}\Delta x_{i,j} + \sum_{k=1}^{m} b_{i,k}\Delta y_{i,k}$$

$$= \mu_i + \sum_{j=1}^{n} a_{i,j}\left(\Delta x_{i,j,wd} + \Delta x_{j,dd}\right) + \sum_{k=1}^{m} b_{i,k}\left(\Delta y_{i,k,wd} + \Delta y_{k,dd}\right)$$

where Δx_i is normally distributed, and Δy_i is a *probabilistic interval variable* that mean and variance are available.

- **Path delay**

$$D^j = \sum_{i \in P_j} \left(\mu_i + A_i^T X_{i,wd} + A_i^T X_{dd} + B_i^T Y_{i,wd} + B_i^T Y_{dd}\right)$$

$$= \underbrace{\sum_{i \in P_j} A_i^T X_{i,wd} + \left(\sum_{i \in P_j} A_i^T\right) X_{dd}}_{D_R^{\ j}} + \underbrace{\sum_{i \in P_j} B_i^T Y_{i,wd} + \left(\sum_{i \in P_j} B_i^T\right) Y_{dd} + \sum_{i \in P_j} \mu_i}_{D_{PI}^{\ j}}$$

Path delay due to Gaussian variables

Path delay due to probabilistic interval variables

Decomposition of Path Delay Function

- Computing distribution due to Gaussian variables (${D_R}^j$) is straightforward
- Focus on path delay due to probabilistic interval uncertainty

$$D_{PI}{}^j = \sum_{i \in P_j} (\mu_i + u_i)$$

where $u_i = B_i^T Y_{i,wd} + B_i^T Y_{dd}$

- Range of delay variation

$$u_i \in \left[\sum_{k=1}^{m} b_{i,k} \underline{\Delta y_{i,k}}, \sum_{k=1}^{m} b_{i,k} \overline{\Delta y_{i,k}} \right]$$

- Mean and variance of path delay

$$E[D_{PI}^j] = \sum_{i \in P_j} \mu_i$$

$$Var\left\{D_{PI}^j\right\} = \sum_{i \in P_j} B_i^T \Sigma_{i,wd} B_i + \left(\sum_{i \in P_j} B_i^T \right) \Sigma_{dd} \left(\sum_{i \in P_j} B_i \right)$$

Computation of Probabilistic Bounds for Path Delay

- Compute probabilistic bounds for a set of distributions satisfying constraints of range, mean, and variance
  - Optimization problem

- Analytical expressions for CDF bounds: a generalization of Chebyshev and Cantelli inequalities (Ferson *et al*, ’02)

$$
\begin{array}{ll}
P(X \le x) = 0 & x < \mu + \sigma^2 / (\mu - \overline{X}) \\
P(X \le x) \ge 1 - (m(1+y) - s^2 - m^2)/y & \mu + \sigma^2/(\mu - \overline{X}) \le x \\
 & \text{and} \quad x < \mu + \sigma^2/(\mu - \underline{X}) \\
P(X \le x) \ge 1/(1 + \sigma^2/(x-\mu)^2) & \mu + \sigma^2/(\mu - \underline{X}) \le x < \overline{X} \\
P(X \le x) = 1 & \overline{X} \le x
\end{array}
$$

where $y = (x - \underline{X})/(\overline{X} - \underline{X})$ $m = (\mu - \underline{X})/(\overline{X} - \underline{X})$ and $s^2 = \sigma^2/(\overline{X} - \underline{X})^2$

- Probabilistic bounds for total path delay ($D_R{}^j + D_{PI}{}^j$) can be computed by convolution

$$CDF(D^j) = CDF(D^j_{PI}) \otimes PDF(D^j_R)$$

Circuit Delay Computation

- **Path-based circuit timing analysis**

$$
\begin{aligned}
D_{\max} &= \max(D^1, \ldots, D^N) \\
&= \max\left(D_R^1 + D_{PI}^1, \ldots, D_R^N + D_{PI}^N \right) \\
&\le \underbrace{\max\left(D_R^1, \ldots, D_R^N \right)}_{D_{R\max}} + \underbrace{\max\left(D_{PI}^1, \ldots, D_{PI}^N \right)}_{D_{PI\max}}
\end{aligned}
$$

- **Delay due to Gaussian variables:** $D_{R\max} = \max\left(D_R^1, \ldots, D_R^N \right)$
  - **Can be computed by SSTA based on first-order delay model and normal assumption**

- **Delay due to interval uncertainty:** $D_{PI\max} = \max\left(D_{PI}^1, \ldots, D_{PI}^N \right)$
  - **Can be bounded if mean and variance are available**
  - **Monte Carlo technique is used**

Robust Monte Carlo Technique

- Monte Carlo techniques are used in timing analysis (Hitchcock ’82; Jyu ’93)
  - Generates samples drawn from given distributions
- Challenge: parameters with unknown distributions
  - Heuristically generates samples of various distributions
  - Time consuming
- Robust Monte Carlo technique is needed
  - Generates samples following *specific distributions* that cause extreme values of target function
- Circuit delay due to probabilistic interval uncertainty is a non-negative convex function
  - Allows to devise a technique for robust Monte Carlo

Convexity of Maximum Path Delay

- **Path delay is linear thus convex function of probabilistic interval variables** (y_i)

$$D_{PI}^{j} = \sum_{i \in P_j} (\mu_i + B_i^T Y_{i,wd} + B_i^T Y_{dd})$$

- **If** $D_{PI}^1, \ldots, D_{PI}^N$ **are convex, their pointwise maximum is also convex**

$$D_{PI\max}(Y) = \max\left(D_{PI}^1(Y), \ldots, D_{PI}^N(Y) \right)$$

- **Gate delays are always positive: non-negativity of maximum path delay**

Robust Monte Carlo Simulation

- Let $\{v_1,\ldots,v_M\}$ be a set of *independent* random variables, where $v_i \in [\underline{v_i}, \overline{v_i}]$, and $E[v_i] = E_i$ for *i*=1 to *M*. Let $y = f(v_1,\ldots,v_M)$ be a ***non-negative convex*** function of the random variable v_i, for *i*=1 to *M*.
- Among all possible *cdfs* of $\{v_1,\ldots,v_M\}$ that correspond to the range and the mean, **the k^{th} moment of the function**, $E[y^k]$, achieves the maximum value when each random variable v_i follows the 2-point distribution:

$$P(v_i = \underline{v_i}) = \underline{p_i}$$

$$P(v_i = \overline{v_i}) = \overline{p_i}$$

where $\overline{p_i} = \dfrac{E_i - \underline{v_i}}{\overline{v_i} - \underline{v_i}}$ and $\underline{p_i} = \dfrac{\overline{v_i} - E_i}{\overline{v_i} - \underline{v_i}}$.

- Furthermore, $E[y^k]$ achieves the minimum when $P(v_i = E_i) = 1$.
- This theorem and its corollary allow us to bound mean and variance of $y = f(v_1,\ldots,v_M)$ using generated samples.

Algorithm of Fast Robust Monte Carlo Simulation

for i **= 1..*N***

Generate samples for die-to-die components

for **each gate**

Generate samples for within-die components

Compute gate delay

end

Compute circuit delay, D_i **.**

end

Compute sample mean and variance,

$$\overline{D} = \sum_{i=1}^{N} D_i \Big/ N$$

$$s_D^2 = \sum_{i=1}^{N} (D_i - \overline{D})^2 \Big/ N - 1$$

With $\overline{D}$**,** s_D^2 **, and range of circuit delay, use generalized Chebyshev inequality to compute lower bound for *cdf*.**

Experimental Setup

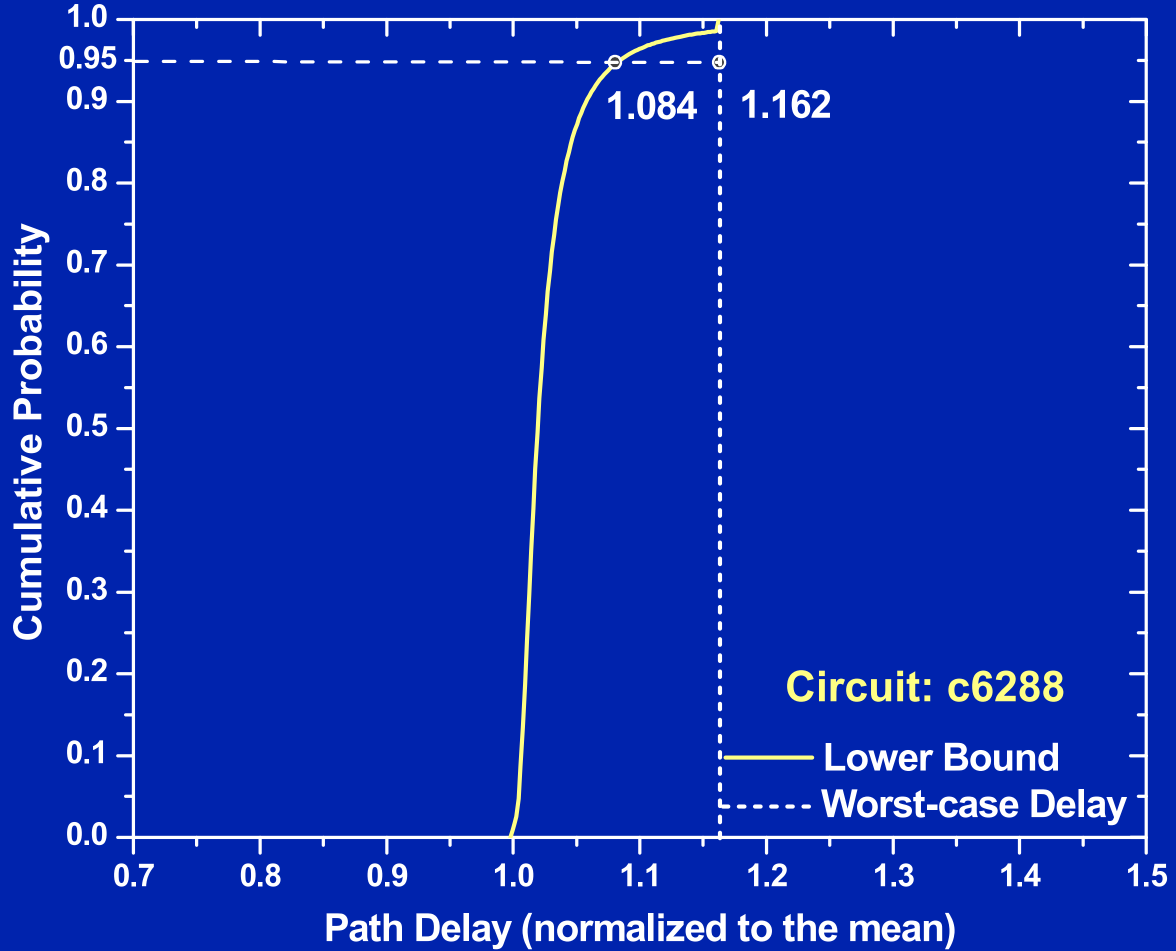
- Path and circuit timing analysis algorithms implemented in C++
- Cell library
  - Characterized using 130nm BPTM technology
- Process uncertainty

Parameter	Modeling	Magnitude of Uncertainty $(3\sigma / \mu)$	Magnitude of With-Die Variation
Effective Channel Length	Gaussian	20.0%	50%
Threshold Voltage	Probabilistic Interval	20.0%	50%
Oxide Thickness	Probabilistic Interval	20.0%	50%

- Environmental uncertainty

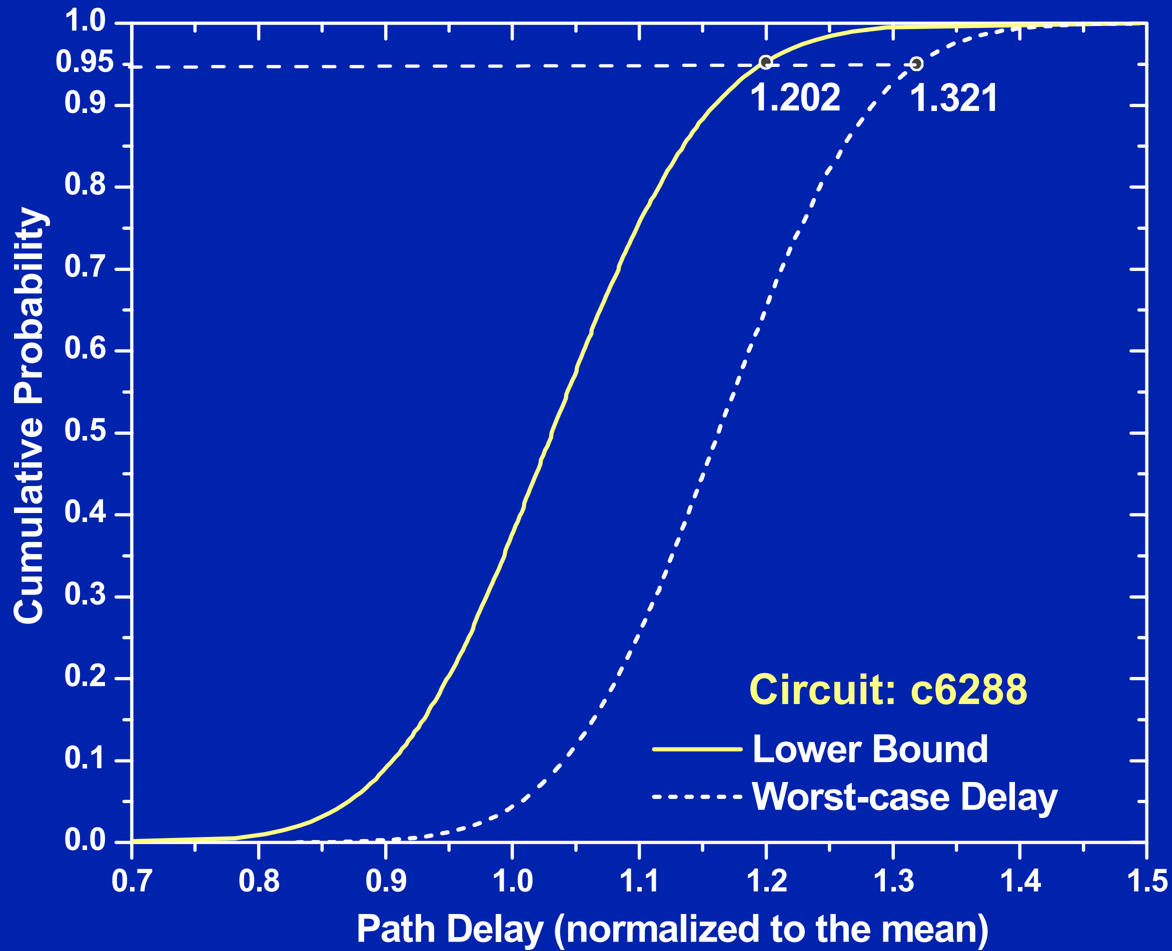
Parameter	Modeling	Magnitude of Uncertainty $(3\sigma / \mu)$	Magnitude of With-Die Variation
Power Supply Voltage	Probabilistic Interval	12.5%	100%

Results: Probabilistic Bounds for Path Delay due to Probabilistic Interval Uncertainty



- Proposed algorithm reduces worst-case delay by 6.7% at 95th percentile

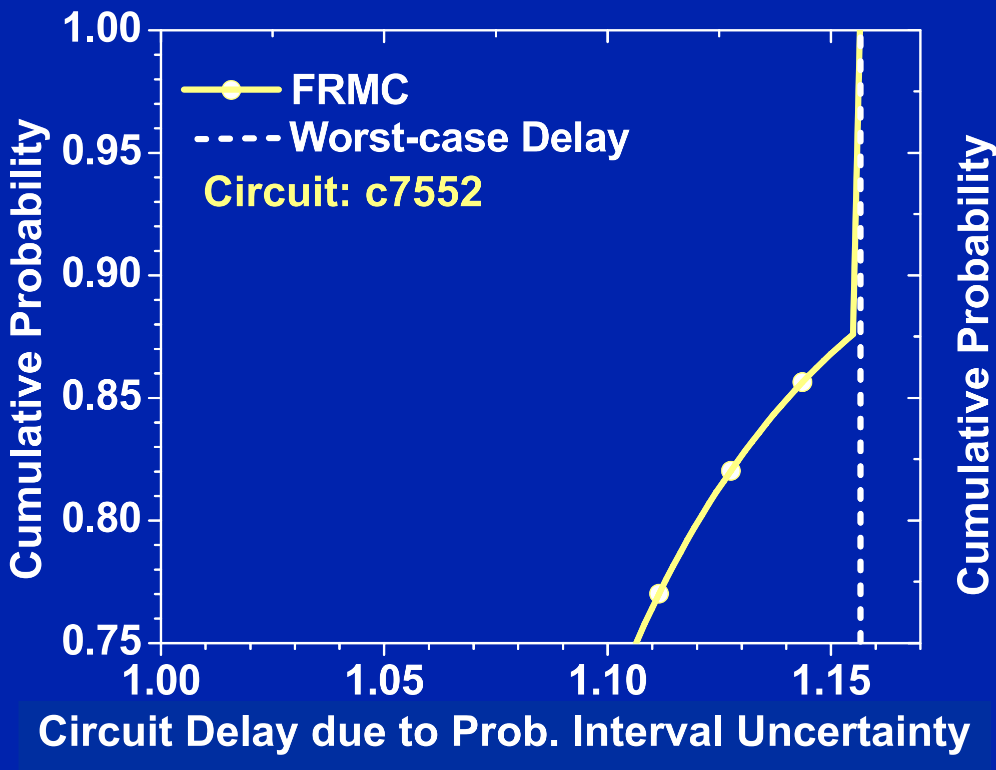
Results: Probabilistic Bounds for Total Path Delay

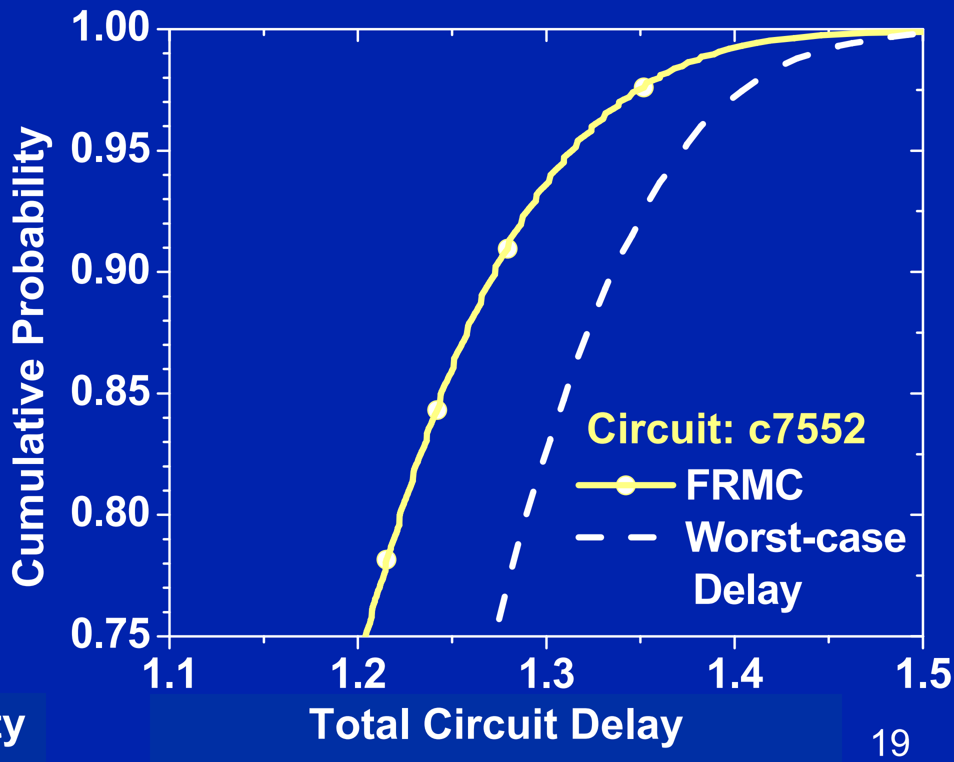


- **Worst-case delay for probabilistic interval uncertainty is added to path delay due to Gaussian variables**
- **Proposed algorithm reduces worst-case delay by 9.0% at 95th percentile**

Results: Probabilistic Bounds for Circuit Delay

- FRMC gives a better bound than worst-case delay at lower than 87th percentile for circuit delay due to probabilistic interval variables.
- For total circuit delay, FRMC improves worst-case delay by 4% at 95th percentile.





Comparison of FRMC and Worst-case Delay

- For total circuit delay, FRMC improves worst-case delay, on average, by 4% at 95th percentile across ISCAS 85 benchmark.

Circuit	Number of Gates	Fast Robust Monte Carlo Simulation					Worst-case Delay for Probabilistic Interval Variables	
		90th Percentile		95th Percentile		Run Time (s)	90th Percentile	95th Percentile
		Delay (ps)	Reduction	Delay (ps)	Reduction		Delay (ps)	Delay (ps)
c880	456	2383	5.62%	2467	4.97%	12	2525	2596
c1355	605	2264	4.59%	2335	4.26%	18	2373	2439
c1908	975	2820	5.56%	2919	4.89%	26	2986	3069
c2670	1544	3124	5.65%	3232	5.08%	38	3311	3405
c3540	1787	4097	5.49%	4237	4.94%	52	4335	4457
c6288	2448	17547	5.28%	18081	4.82%	87	18526	18996
c5315	2600	3579	5.49%	3703	4.88%	79	3787	3893
c7552	3874	3136	4.88%	3236	4.46%	114	3297	3387

Conclusion and Future Work

- New strategy of handling uncertainty
  - Permits handling parameters of incomplete information
  - Reduces over-conservatism of worst-case timing analysis that only uses interval information of parameters
  - Predicts probability of timing violation for circuits with error correction mechanism
  - Also compatible with SSTA based on first-order delay model and normal assumptions
- Future: experiments on real-life cases and circuits